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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,149	11/24/2003	Taqi N. Buti		1148

30449 7590 12/12/2006

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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,149	BUTI ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,15-21 and 30* is/are rejected.

7)☒ Claim(s) *7-14 and 22-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 6, 15 – 21 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger et al. (US Patent Number 6,243,287 hereinafter "Naffziger") in view of Favor (US Patent Number 5,819,056).

3. As per claims 1 and 16, Naffziger teaches a memory buffer comprising: a physical memory array (SRAM) partitioned into multiple physical and identical memory sub-arrays arranged in sequential order from a first memory sub-array to a last memory sub-array (identical physical sub-array groups 0 – 7 of figure 4a and 4b), each memory sub-array having multiple physical memory entry positions and adapted to store a different memory of a set of concurrent memory (memory cells) in a single memory (memory cell) entry position of any one of said memory sub-arrays, said set of concurrent memory arranged in sequential order from a first memory cell to a last memory cell (structure is comprised of sequential groups of memory cells organized with wordlines in an SRAM array, column 2, lines 7 – 34, figures 2 - 4).

Naffziger does not explicitly teach the memory data being instruction data.

Favor teaches a system in which instructions are stored in a memory (figure 5).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to store the instructions of Favor in the memory cells of Naffziger. One of ordinary skill would be motivated to make such modification in order to enhance processors task of decoding in a memory based architecture (column 1, lines 50 – 56).

4. As per claims 2 and 17, Favor teaches an instruction buffer wherein: each instruction of said set of concurrent instructions is stored in a different memory sub-array and the set of concurrent instructions may wrap (pointer is defined as point to the next instructions in the order represented by the arrow, column 34, lines 27 – 36) from said last memory sub-array to said first memory sub-array (pointer wrapping around from element 514 to element 522 of figure 5).

5. As per claims 3 and 18, Favor teaches an instruction buffer wherein when said set of concurrent instruction wraps around, each instruction that is wrapped is written to an instruction entry position in a corresponding memory sub-array that is one instruction entry position higher (position of element 522 is entry position higher than element 514 of figure 5) in a memory sub-array corresponding to each instruction that is not wrapped except an instruction wrapped from the last instruction entry position of the last memory sub-array wraps to the first instruction entry position of the first memory sub-array (in the condition of the pointer of element 534 wrapping around to element 512 the entry position would be lower at 512 than 534).

6. As per claims 4, 5, 19 and 20, Naffziger teaches an instruction buffer wherein each memory sub-array comprises single write port and single read port memory cells (data is written to and read from each of the SRAM cells via connections 15a and 15b, figure 1, column 4, lines 7 – 16).

7. Naffziger modified by the teachings of Favor as applied in claim 1 above, as per claims 6 and 21, Naffziger teaches an instruction buffer wherein: each instruction entry position is defined by a physical instruction entry position (memory address, column 6, lines 25 – 27) and a corresponding logical instruction entry position (address wordlines, column 6, lines 25 – 27), each logical instruction entry position in a particular memory sub-array is a fixed number higher than an immediately previous logical instruction entry position in said particular memory sub-array; said physical instruction entry positions in each memory sub-array are one logical instruction entry position higher than corresponding physical entry positions of a immediately previous memory sub-array, the first physical instruction entry position and first logical instruction entry position of a first memory sub-array being the same; and each said instruction of said set of concurrent instructions is stored in consecutive logical instruction entry positions of said memory array (all internal components are number via rows, columns, cells groups in a low to high numerical method, groups are shown number 0 – 7 in figure 3, and an n x m SRAM array is further taught) .

8. As per claims 15 and 30, Favor teaches an instruction buffer wherein each memory sub-array is selected from the group consisting of static random access memory arrays (SRAM, column 3, lines 64 – 67), dynamic random access memory arrays (DRAM, column 1, lines 13 – 15), latch arrays (column 5, lines 3 – 4), or a register array (1-D array, column 4, lines 4 – 6).

Response to Arguments

9. Applicant's arguments with respect to claims 1 – 6, 15 – 21 and 30 have been considered but are moot in view of the new ground(s) of rejection necessitated by amendment.

10. Fully considering Applicant's arguments with respect to claims 7 and 22 and upon further consideration in light of the new grounds of rejection, claims 7 and 22 contain allowable subject matter.

11. Claims 8 – 14 and 23 – 29 depend from claims 7 and 22 and thus contain allowable subject matter.

12. Claims 7 – 14 and 22 – 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is an examiner's statement of reasons for allowable subject matter: the prior art on the record teaches certain aspects of the current application.

Naffziger teaches a multiplexer adapted to receive data from consecutive sub-arrays with an N:1 multiplexer, N being the number of concurrent sub-arrays as seen in figure 4. Naffziger further contains wordline decoders further directed as selects for the multiplexer.

However the prior art fails to teach or suggest alone or in combination the limitations a rotator multiplexer adapted to direct instructions to an entry position in different consecutive memory sub-arrays and an output multiplexer adapted to order a sequence of instructions read out of a memory array to match the order of instructions in combination with the independent claims. Prior art is further silent on motivation to combine such features and functionality and is therefore deemed allowable subject matter.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571)272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

KIM HUYNH
SUPERVISORY PATENT EXAMINER
12/8/06